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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
JUNTIMA, NITTAYA	

ART UNIT	PAPER NUMBER
2663	6

DATE MAILED: 05/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/737,646	BREWER ET AL.
	Examiner	Art Unit
	Nittaya Juntima	2663

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-10,17-37* is/are rejected.

7)☒ Claim(s) *2,11-16 and 38-47* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2,5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

- the status of all patent applications referenced in the specification should be updated.

Appropriate correction is required.

Claim Objections

2. Claims 1, 20, 33, and 39 are objected to because of the following informalities:

- in claim 1, line 6, "ASIC " should be spelled out as "application specific integrated circuit" and

line 9, "RAM" should be spelled out as "random access memory" to avoid any confusion, and "memory" should be deleted;

- in claim 20, lines 2-3, "the maximum" should be changed to "a maximum;"

- in claim 33, line 2, "each of" should be added after "to" and "packet" should be changed to "packets;" and

- in claim 39, lines 5, 9, and 10, "39-a", "39-b" , and "39-c" should be changed to "a", "b", and "c," respectively, to avoid any confusion.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1** and **3-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Crocker et al. (USPN 6,351,454 B1).

Per **claim 1**, as shown in Figs. 2 and 4, Crocker et al. teach a system (the data exchanged system 10 in Fig. 1), ***a packet forwarding engine*** (transmitting agent 12), ***a plurality of fast data paths*** (two data connections connecting a transmitting queue 32 to transmit link queues 50 and 60), ***input ports*** (input ports on transmit link queues 50 and 60 for receiving data from a transmitting queue 32), ***output ports*** (two output ports on transmitting queue 32 for transmitting data to transmit link queues 50 and 60), ***a processing block*** (transmitting queue 32), ***a plurality of rate matching queues*** (packet memories 34-48 supporting variable packet lengths), ***an ingress*** (receiving agent 18), ***a packet ordering block*** (receiving queue 70), ***a plurality of reorder queues*** (packet memories 72-86), ***a packet data memory*** (receive link queue 51 which comprises memories 53-59). See col. 4, lines 26-33, col. 5, lines 21-50, and col. 7, lines 52-col. 8, lines 1-3, col. 9, lines 32-58.

However, Crocker et al. fail to teach an ingress is an ASIC and a packet data memory is a RAM.

It would have been obvious to include an ASIC and RAM into the teaching of Crocker et al. such that an ingress (a receiving agent 18) would be made of an ASIC and a packet data memory (receive link queue 51) would be made of a RAM. The suggestion/motivation to do so

would have been to provide (i) a custom-designed circuit in a large production volume for an ingress and (ii) a fast and accessible data storage medium for a packet data memory by using an ASIC RAM, respectively.

Per **claim 3**, since Crocker et al. teach that each of the transmit link queues 50 and 60 has memories to support packet of variable size (col. 5, lines 34-59, see also col. 1, lines 62-col. 2, lines 1-5 and col. 8, lines 27-32), therefore, it is inherent that the input ports of the packet forwarding engine (the transmitting agent 12) must include a wide bandwidth port and a narrow bandwidth port when transmitting wide bandwidth packets and narrow bandwidth packets, respectively.

Per **claims 4** and **5**, Crocker et al. do not teach that the wide bandwidth port has a capacity of approximately 3.2 Gb/s and the narrow bandwidth port has a capacity of approximately 1.6 Gb/s. However, it would have been obvious to one skilled in the art to incorporate the wide bandwidth port of a capacity of approximately 3.2 Gb/s and the narrow bandwidth port of a capacity of approximately 1.6 Gb/s into the teaching of Crocker et al. The suggestion/motivation to do would have been to accommodate different high bandwidth demands and provide system scalability since providing different bandwidth ports only involves routine skill in the art.

Per **claim 6**, an exception reorder queue is not defined, therefore, reads on a memory, e.g. memory 72, included in the reorder queues (packet memories 72-86). See Fig. 4 and col. 7, lines 64-65.

Per **claim 7**, although Crocker et al. teach that packets are moving from RLQs into the packet ordering block (receiving queue 70) in order of sequence numbers (col. 9, lines 19-40,

see also col. 8, lines 17-26), Crocker et al. fail to teach that the packet ordering block contains a now serving counter. However, it would have been obvious to one skilled in the art to include a now serving counter into the packet ordering block (receiving queue 70) of Crocker et al. to enable the packet ordering block to internally keep tract of the sequence numbers of the packets received.

Per **claims 8-10**, Crocket et al. teach that data of variable lengths that is ready for transmission is located in the processing block (transmitting queue 32, Fig. 2) (col. 5, lines 25-33), but fail to teach that the processing block is interconnected with an input data link having a bandwidth capacity of approximately 10Gb/s, and multiple input data links, each has a bandwidth of at least 1.0 Gb/s or 2.5Gb/s. However, it would have been obvious to one skilled in the art to include an input data link of 10Gb/s and multiple input data links, each with at least 1.0 Gb/s or 2.5 Gb/s, into the teaching of Crocker et al. The motivation/suggestion to do so would have been to provide and support variable input data bandwidths to the processing block (transmitting queue 32) and providing bandwidths of 10, 2.5 and 1.0 Gb/s only involves routine skill in the art.

5. **Claims 17-25, 28-29,** and **33-37** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fawaz et al. (USPN 6,654,374 B1) in view of Hirome (USPN 5,309,435).

Per **claim 17**, as shown in Fig. 6, Fawaz et al. teach receiving through ***an input data link*** (input data link connecting input buffer 302 to classifier 304) ***the packets*** (packets, e.g. Ethernet frames), distributing the packets among ***a plurality of rate matching queues*** (SLA buffers 306-312), such that each rate matching queue feeds one of substantially ***parallel data links*** (data links connecting SLA buffers 306-312 to the scheduler 316) having ***differing information rates*** (data

links between SLA buffers 306-312 support differing packet SLAs having differing bandwidths), flowing the packets through the plurality of substantially parallel data links at differing information rates, and reordering the packets after the flowing (col. 7, lines 28-32, 47-60, see also col. 6, lines 62-col. 7, lines 1-5).

However, Fawaz et al. fail to teach sequence numbering the packets.

Hirome teaches sequence numbering packets (Fig. 7 PH/sequence generator generates the sequential number to be added to each of the header of packets generated by the packet generator 51, col. 7, lines 1-6).

Given the teaching of Hirome, it would have been obvious to one skilled in the art to include sequence numbering packets into the teaching of Fawaz et al. The suggestion/motivation to do so would have been to provide a reliable transmission system as taught by Fawaz et al. (col. 1, lines 65-col. 2, lines 1-12).

Per **claim 18**, Fawaz et al. teach that the substantially parallel data links (data links connecting SLA buffers 306-312 to the scheduler 316) support different SLAs (col. 7, lines 47-60), but fail to teach that they are limited to a maximum packet flow rate of approximately 21. million packets per second. However, it would have been obvious to one skilled in the art to modify the teaching of Fawaz et al. so that the substantially parallel data links (data links connecting SLA buffers 306-312 to the scheduler 316) would be limited to a maximum packet flow rate of approximately 2.1 million packets per second. The suggestion/motivation to do so would be to accommodate a SLA with a maximum packet flow rate, e.g. 2.1 million packets per second, because such modification involves only one routine skill in the art.

Per **claim 19**, Fawaz et al. teach that ***a portion of the substantially parallel data links*** (a portion of data links connecting SLA buffers 306-312 to the scheduler 316) are narrow bandwidth data links, e.g. some of the links support 128 kbps connection between two nodes A and B (col. 6. lines 67-col. 7, lines 1-5).

Per **claim 20**, Fawaz et al. teach that ***a portion of the substantially parallel data links*** (a portion of data links connecting SLA buffers 306-312 to the scheduler 316) are wide bandwidth data links, such that a maximum bandwidth limit of the wide bandwidth data links is greater than a maximum bandwidth limit of the narrow data links (the system in Fig. 6 is operating in nodes 102 and 106 which operate at various rates, e.g. 10 Mbps 100Mbps or even 1Gbps, col. 6, lines 25-34, and support different SLAs, therefore, it is inherent that some of the data links between SLA buffers 306-312 and the scheduler 316 must support the wide bandwidth data links as recited in the claim).

Per **claims 21-22** and **24**, Fawaz et al. teach processing the packets within each of the plurality of substantially parallel data links (processing is not further defined, therefore, reads on packets being transmitted on the data links from the SLA buffers 302-312 to the scheduler 316, col. 7, lines 47-60), but fail to explicitly teach that (i) the maximum bandwidth of the narrow bandwidth data links is approximately 1.6 Gb/s, (ii) the maximum bandwidth of the wide bandwidth data links is approximately 3.2 Gb/s, and (iii) the processing is limited to a maximum data rate of approximately 2.5 Gb/s. However, it would have been obvious tot one skilled in the art to modify the teaching of Fawaz et al. such that (i) the maximum bandwidth of the narrow bandwidth data links is approximately 1.6 Gb/s, (ii) the maximum bandwidth of the wide bandwidth data links is approximately 3.2 Gb/s, and (iii) the processing is limited to a maximum

data rate of approximately 2.5 Gb/s because such modifications involve only routing skill in the art.

Per **claim 23**, Fawaz et al. teach that the packets are received through the input data link (input data link connecting input buffer 302 to classifier 304) at a rate of approximately 10 Gb/s (nodes 102 and 106 shown in Fig. 6 when operate at OC-192 receive packets at a rate of 9.953280 Gb/s or approximately 10Gb/s, col. 6, lines 26-34).

Per **claim 25**, since Fawaz et al. teach that each packet is classified according to its SLA, i.e. minimum bandwidth, and placed into a buffer 306-312 that corresponds to the SLA, col. 6, lines 62-67 and col. 7, lines 28-31 and 47-53), therefore, it is inherent that the packets are distributed among the matching queues (SLA buffers 306-312) according to packet size, such that large packets greater than a threshold size are placed in large packet queues feeding wide bandwidth data links (corresponding data links connecting corresponding high SLA buffers to the scheduler 312) and such that small packets not greater than the threshold size are placed in small packet queues feeding narrow bandwidth data links (corresponding data links connecting corresponding lower SLA buffers to the scheduler 312).

Per **claim 28**, Fawaz et al. teach that small packet and large packet are placed in a particular small packet queue and particular large packet queue, respectively (packet is placed into a SLA buffer according to its minimum bandwidth requirement, col. 7, lines 47-53, see also col. 6, lines 62-67). However, the combined teaching of Fawaz et al. and Hirome does not teach that the packets are distributed roughly equally among the rat matching queues (SLA buffers 306-312) using a round robin algorithm. However, it is well known that a round robin algorithm is used to provide fairness in a queuing system. Therefore, it would have been obvious to one

skilled in the art to distribute the packets roughly equally among the rate matching queues (SLA buffers 306-312 in Fig. 6 of Fawaz et al.) using a round robin algorithm in order to provide fairness to the rate matching queues.

Per **claim 29**, although Fawaz et al. teach that each SLA buffer 306-312 supports packets with different bandwidth requirements (col. 7, lines 47-53), Fawaz et al. do not teach that the threshold size is approximately 200 bytes. However, it would have been obvious to one skilled in the art to set a threshold size to be any integer, e.g. 200 bytes, in order to classify the small and large packet sizes (SLAs) as such setting only involves routine skill in the art.

Per **claim 33**, Fawaz et al. fail to teach that the sequence numbering is applied within a header prepended to the packet. However, Hirome teaches that the sequence numbering is applied within a header prepended to each of the packets (col. 7, lines 1-6).

Per **claim 34**, Fawaz et al. teach that the packets comprise fast path packets and exception packets different from the fast path packets (fast path and exception packets are not further defined, therefore, read on different packets with different SLAs are supported, col. 6, lines 62-col. 7, lines 1-5 and 39-53).

Per **claim 35**, Fawaz et al. teach that the exception packets are distinguished from the fast path packets by setting a bit within a header prepended to each packet (each packet is classified according to its SLA using information contained in the header such as a source packet switch, a destination switch, or the type of application, col. 7, lines 39-46).

Per **claim 36**, Fawaz et al. teach that the exception packets are processed within a portion of ***the plurality of substantially parallel data links*** (data links connecting SLA buffers 306-312 to the scheduler 316) that is bypassed by ***the fast path packets*** (packets are transmitted from each

SLA buffer 306-312 to the scheduler 316 on the corresponding data links connecting the two elements, col. 7, lines 47-60, therefore, SLA-1 and SLA-2 packets are transmitted on the links connecting SLA-1 and SLA-2 to the scheduler 316 which are bypassed by SLA-3 packets).

Per **claim 37**, it is inherent that ***the exception packets*** (for example packets of SLA-1 and SLA-2) are reordered separately and independently from ***the fast path packets*** (for example packet of SLA-3) since the packets are classified and routed to and received by their corresponding destinations using their destination identifiers and scheduled for transmission by the scheduler 316 (col. 7, lines 28-39 and 54-60).

6. **Claims 26-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fawaz et al. (USPN 6,654,374 B1) in view of Hirome (USPN 5,309,435), and further in view of Crocker et al. (USPN 6,351,454 B1).

Per **claims 26** and **27**, Fawaz et al. teach that small packet and large packet are placed in a particular small packet queue and particular large packet queue, respectively (packet is placed into a SLA buffer according to its minimum bandwidth requirement, col. 7, lines 47-53, see also col. 6, lines 62-67). However, the combined teaching of Fawaz et al. and Hirome does not teach that the small packet is placed in a particular small packet queue having the greatest unoccupied space and the large packet is placed in a particular large packet queue having the greatest unoccupied space.

Crocker et al. teach placing a packet into a queue TLQB 60 in Fig. 2 that is less full (col. 6, lines 6-16).

Given the teaching of Crocker et al., it would have been obvious to one skilled in the art to include placing a packet into a queue that is less full into the combined teaching of Fawaz et

al. and Hirome such that the small packet is placed in a particular small packet queue having the greatest unoccupied space and the large packet is placed in a particular large packet queue having the greatest unoccupied space. The suggestion/motivation to do so would have been to provide efficient bandwidth allocation as taught by Crocker et al. (col. 6, lines 6-9).

7. **Claims 30-32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fawaz et al. (USPN 6,654,374 B1) in view of Hirome (USPN 5,309,435), and further in view of Valko (USPN 6,519,248 B1).

Per **claim 30,** Fawaz et al. teach a narrow bandwidth data link (Fig. 6, a data link connecting one of the SLA buffers 306-312 to the scheduler 316 that supports a 128 kbps connection between two nodes A and B, col. 6. lines 67-col. 7, lines 1-5).

The combined teaching of Fawaz et al. and Hirome does not teach inserting a keep-alive packet into any narrow bandwidth data link that is idle for a predetermined period of time.

However, Valko teaches inserting a keep-alive packet into a wireless link that is idle for a predetermined period of time in an analogous art, i.e. wireless communication (keep alive packets are sent to the attached base station Fig. 1 over idle communication link every T_{ka} period, col. 16, lines 39-55).

Given the teaching of Valko, it would have been obvious to one skilled in the art to include inserting a keep-alive packet into the combined teaching of Fawaz et al. and Hirome such that a keep–alive packet would be inserted into any narrow bandwidth data link that is idle for a predetermined period of time. The motivation/suggestion to do would have been to inform the corresponding party, i.e. the scheduler 316 of Fawaz et al., that the link is still reachable and alive as taught by Valko (col. 16, lines 39-41 and 47-50).

Per **claims 31** and **32,** the combined teaching of Fawaz et al., Hirome, and Valko does not teach that the predetermined period of time is programmable and on the order of 10 microseconds.

It would have been obvious to one skilled in the art to modify the combined teaching of Fawaz et al., Hirome, and Valko such that the predetermined period of time is programmable and on the order of 10 microseconds as it involves only routine skill in the art and does not give any unexpected results.

Allowable Subject Matter

8. Claims 2 and 11-16, and 38-47 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nittaya Juntima whose telephone number is 703-306-4821. The examiner can normally be reached on Monday through Friday, 8:00 A.M - 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on 703-308-5340. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nittaya Juntima
May 4, 2004

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